CERTIFICATION

I, the undersigned, am a professional translator, fully competent to translate from German into English, and I declare hereby that the attached English rendition of the International Patent Application PCT/DE03/04286 entitled

METHOD FOR THE PRODUCTION OF A SEMICONDUCTOR

is a genuine translation, accurate in every particular, to the best of my ability and knowledge.

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Method For the Production of a Semiconductor Component

Technical Background

The present invention relates to a method for the production of a semiconductor component comprising at least one first vertical power component and at least one lateral, active component and/or at least one second vertical power component as well as to a semiconductor component produced therewith.

Prior Art

Monolithic integration is a method of producing microchips in which the different components do not need to be adjusted and glued on individually, but rather the entire chip is produced in one piece. Apart from requiring less adjustment, such systems are unusually robust.
Power components, in particular bipolar stages and MOS stages for processing higher currents ($I > 1$ amperes) with stray powers of $P_V > 5$ watts, have been available for monolithic integration for some time. Today these components reach powers up to 1 kW, respectively currents up to 50A.

Increasingly finding use in such concepts are drive circuits to activate the power stages and protective circuits to protect against thermal and electric overload. Finally even information processing has been included in the integration concept.

Such integrated circuits, which contain an information processing circuit component in addition to a power component on the chip are referred to as so-called smart power circuits.

Using these smart power circuits has both process-specific as well as component-specific advantages and disadvantages. Advantageous is in any case to have a bipolar process, a CMOS process and a PMOS process, in particular for MOS power stages with vertical current flow available on the chip. Such Bipolar, CMOS, PMOS and even BCD concepts are continuously being further developed.

Monolithic integration of the aforementioned power components is realized in various manners dependent on the voltage class. So-called smart power processes, such as BCDMOS, are used for voltages up to some 100 V. Lateral separation of different sections occurs either by doping regions or by dielectric insulation.

In vertical power semiconductors, insulation of the power components from the control circuit is usually achieved by means of a pn-junction. The problem with such a pn-junction, however, is that between the source drain zones of the n-

channel transistor and the source-drain zones of the p-channel transistor, there is a thyristor structure which can ignite and thus can impair the operation of the inverter, respectively destroy the component. This undesirable effect is referred to as the 'latch-up effect". The higher the desired degree of integration, the closer one tries to arrange the p-channel and n-channel structure, and the more effective this disturbing factor becomes.

For this reason, various processes based on a dielectric insulation of the different components of the circuit from each other have been developed. For example, instead of the pn-junction, the corresponding power component can also be insulated from the control circuit with the aid of dielectric insulation. The drawback of this type of insulation is that presently these approaches to monolithic integration of power components are still based on the extremely expensive silicon-on-insulator technology (SOI). In order to insulate the different components, trenches are etched to the buried oxide layer, and these trenches have to be filled with oxide or oxide and polysilicon.

A fundamental disadvantage of SOI technology is that an undesired control effect of the substrate is unavoidable. The substrate acts over the buried insulator like a second gate electrode on the transistors, the second gate electrode being integrated in a layer. If differences in potential occur between the substrate and the corresponding layer, this can lead to shifts in the threshold voltage and changes in the switching state of the transistors.

In this context, DE 42 01 910 A1 presents a further development. This printed publication describes a method for producing an integrated circuit having at least two vertical power components. The object of the method is to largely avoid switching procedures of a vertical power component influencing the control circuit, respectively a second vertical power component. The semiconductor element described in this printed publication is essentially distinguished by the control circuit lying above an etch recess on the rear side and being delimited from the etch recess by an etch stop layer. Moreover, the control circuit is insulated in lateral direction from the power components by a LOCOS insulation. A drawback of the power component described in this printed publication, however, is, firstly, that very much silicon surface is required for the lateral insulation regions and, secondly, that semiconductor components that are suited for this type insulation are not suited for higher voltage classes.

Based on the prior art, the object of the present invention is to provide a semiconductor component and a method for the

production thereof that permit cost-effective integration of a vertical power component and a lateral, active component and/or additional vertical power components. In particular, with the aid of a component that solves the aforementioned object, it should be possible to integrate power components of higher voltage classes on the semiconductor component.

The object is solved with the method according to claim 1 and the semiconductor component according to claim 10. Advantageous further developments of the inventive concept are the subject matter of the subordinate claims and described in the following description with reference to the preferred embodiments.

According to the present invention, provided is a method for the production of a semiconductor component comprising a first vertical power component and at least one lateral, active component and/or at least one second vertical power component with the following steps:

- provision of a silicon substrate having a front side and a back side,
- etching at least one trench which completely encompasses at least one part surface of the front side in the silicon substrate,
- filling up the at least one trench with an insulation which contains at least one dielectric or is a dielectric,
- conducting process steps on the front side of the silicon substrate in order to produce a first vertical power component and at least one lateral, active component and/or at least one second vertical power component in such a manner that both the first power component and the at least one lateral, active component and/or the one second vertical power component are arranged on the substrate concentrically or eccentrically around a common point of reference and are separated from each other by the at least one trench,
- thinning the entire surface of the silicon substrate from the back side to the insulation and
- contacting the power components from the back side.

The invented method permits integrating a multiplicity of vertical power components and lateral, active components on a semiconductor component. The electric insulation of the various components is achieved in that first trenches, which are filled with a dielectric, are etched into the silicon wafer. The depth of the trenches is set in such a manner that the depth corresponds to the thickness of the wafer after the thinning process. One or a multiplicity of trenches can be used to insulate the single components.

In a special embodiment of the invented method, the first power component, the at least one lateral, active component and/or the at least one second vertical power component are

designed approximately ring-shaped and/or disk-shaped. Preferably, the lateral, active component is designed disk-shaped and is disposed on the front side in such a manner that it is completely encompassed by the trench in the first power component.

Realized in this manner is a concentric arrangement of the respective functional elements with the interior area of the semiconductor component containing lateral, active components and the power components being arranged toward the outside in rings around the lateral, active component.

In a further development of the invented method it is provided that after the thinning and before the contacting of the at least one power component, a dielectric is deposited on the back side of the substrate. The purpose of the dielectric is to completely electrically decouple the wafer substrate. In order to ensure backside contacting of the power components, in a subsequent process step the dielectric is opened at the corresponding sites for backside metalization.

On the front side of the silicon substrate preferably at least one trench which completely encompasses at least one part area of the front side is etched into the surface. The depth of the at least one trench is set in such a manner that it corresponds to the thickness of the wafer after the thinning process. For reasons of lateral field distribution, combinations of a dielectric and doped polysilicon can be used for filling up the trenches.

In another, particularly suited preferred embodiment of the invented method, a multiplicity of vertical power components and lateral, active components are arranged on a silicon substrate in such a manner that they are arranged concentrically or eccentrically around a common point of reference on the substrate and are insulated from one another by a trench produced by means of the aforementioned method.

Contacting the one power component or the multiplicity of power components preferably occurs using the following steps:

- production of openings in the dielectric for contacting the at least one power component from the back side and
- application of a metalization on the back side.
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In a special further development, the applied metalization is structured.

Another, especially suited preferred embodiment provides that the at least one lateral, active component is placed in a doped trough. In this manner it is ensured that the lateral, active components on the wafer surface are decoupled potentially from the live wafer back side. Preferably, for

this purpose the at least one lateral, active component is placed in a p-doped trough.

Furthermore, particularly suited is to integrate the at least one lateral, active component in Bipolar, CMOS, NMOS and/or PMOS technology in the semiconductor component.

The invented semiconductor is provided with at least one first vertical power component and at least one lateral, active component and/or at least one second vertical power component, between which at least one trench filled with an insulation is placed. The described semiconductor component is distinguished by the insulation being provided with at least one dielectric and by the at least one vertical power component and the at least one lateral, active component being designed approximately ring-shaped and/or disk-shaped and arranged concentrically or eccentrically around a common reference point on the silicon substrate.

Due to the invented executions, the aforementioned semiconductor component permits integrating a multiplicity of vertical power components and lateral, active components on a component. Moreover, an essential advantage of the invented semiconductor is that vertical and lateral, active components are arranged in particularly space saving manner on a component.

Preferably, the invented semiconductor component utilizes power components for voltages of up to 1700 V. Depending on the used power component, the voltage classes vary between 600 and 1700 V. Therefore, it is possible to employ power MOS components in a voltage class of 100 to 200 V, IGBTs in a voltage class of up to 1700 V, preferably of 600 to 1200 V, or diodes as the power component.

In order to prevent high field strengths at the active region in case of blocking, the aforementioned power components need at any rate a edge bordering structure. Thus in components for voltages up to 1200 V, the length of these edge borderings is, for example, up to 600 µm. If the components were placed side by side in a conventional manner on a wafer and separated by a conventionally executed trench insulation, an edge bordering, over which the metalization would have to be led, would be provided for each single component. Contrary to this, the preferably concentric arrangement according to the present invention of the respective functional elements integrated on a semiconductor component greatly reduces the space required for the aforedescribed edge bordering structures. Moreover, this especially suited arrangement of the functional components considerably reduces the complexity of contacting.

In a special preferred embodiment, the power components are arranged in a ring from the inside to the outside. Preferably the at least one lateral, active component is completely encompassed by at least one filled trench and one vertical power component.

Moreover, to ensure that the lateral, active components on the wafer surface are also decoupled potentially from the live back side of the wafer, another special preferred embodiment provides that the at least one lateral, active component is placed in a doped trough.

Furthermore, it is especially advantageous to provide a dielectric on the back side of the semiconductor component in such a manner that a completely electric decoupling is ensured even after thinning the wafer substrate. For backside contacting of the power components, the dielectric is preferably provided with openings.

The invented method for producing a semiconductor component and the semiconductor is made more apparent in the following with reference to the figures described below without the intention of limiting the scope or spirit of the overall inventive idea.

Brief Description of the Invention

The present invention is described in the following using preferred embodiments with reference to the drawings by way of example without the intention of limiting the scope or spirit of the overall inventive idea.

Fig. 1 shows process steps for electric insulation of the components on a wafer,

Fig. 2 shows a concentric arrangement of the functional elements according to the present invention, and

Fig. 3 shows the decoupling of the logic region in the present invention.

Fig. 1 depicts the process steps for electric insulation of the components on a wafer. The electric insulation of the different components is achieved by first etching trenches 2 into the silicon substrate 1. Then in a second process step, the trenches 2 are filled with a dielectric or a combination of a dielectric and polysilicon as the insulation layer 4. After this, the silicon substrate 1 is thinned on the back side to the bottom 3 of the trench 2 etched into the silicon substrate 1. In this manner, the insulation layer 4 filled into the trenches 2 is exposed on the back side. The depth of

the trenches 2 is set in such a manner that it corresponds to the thickness of the wafer after the thinning process.

In contrast, fig. 2 depicts a semiconductor component executed according to the present invention. The respective functional elements 5,6 are arranged concentrically and separated by trench insulations 4 on a substrate. Alternatively, the functional elements 5,6 are arranged eccentrically. The interior area of the chip contains the lateral, active components 6 such as for example components executed using Bipolar, CMOS, NMOS or PMOS technology. The power components 5 such as for example IGBTs and/or diodes are placed in a ring around the lateral, active component 6. Of course, both the power components 5 and/or a lateral, active component 6 can be arranged in such rings about a centrally placed and disc-shaped functional element.

Fig. 3 depicts a sectional view of an invented semiconductor component. Arranged on the semiconductor component are an IGBT 9, a diode 10 and a lateral, active component 6, which are separated from each other in an electrically insulating manner by a trench insulation 4. Provided on the front side is a multiplicity of front side contacts 11 in the form of soldering bumps. Furthermore, the lateral, active component 6 is embedded in a doped trough 12, which is executed as deep p-doping. In this manner, the lateral, active component 6, which is located on the wafer surface, is potentially decoupled from the live back side of the wafer.

Fields occurring are received via the space charge region of the doped trough 12. For complete electrical decoupling, a dielctric 13 is placed on the back side after thinning the wafer substrate. As fig. 3b shows for backside contacting the power components 6, the dielectric 13 is opened at the corresponding sites for backside metallization 8 which is applied on the back side of the semiconductor as the final step.

List of Reference

1 Silicon substrate

2 Trenches

3 Bottom of the trench

4 Insulation layer

5 Power component

6 Lateral, active component

7 Edge bordering structure

8 Metalization

9 IGBT

10 Diode

11 Front side contact

12 Doping trough

13 Dielectric

14 P+ implant

15 n+ implant